University of Colorado - Boulder

ECEN 5730
Practical PCB Design Manufacture — Fall 2024

Lab 5 Report - Switching Noise and Loop Inductance with the Slammer Circuit

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Introduction

In this lab, we will explore the effects of switching noise on a power distribution network (PDN) using a slammer circuit. This type of circuit is designed to simulate the fast transient current demands that occur in real-world integrated circuits (ICs) when performing operations such as driving I/O signals or executing computational tasks. The goal is to build a circuit that will help us visualize the power rail voltage droop and release spikes that result from these fast transients, as well as study how decoupling capacitors can mitigate such noise.

The purpose of this lab is to understand the origin and mitigation of switching noise. We aim to:

- Build and analyze a slammer circuit that demonstrates the switching noise caused by fast current transients.
- Measure the voltage droop on the power rail when there is a large current demand and observe the spike in voltage during the release when the current turns off.
- Investigate how different rise times for current transients affect the amount of switching noise.
- Explore the role of decoupling capacitors in reducing noise and stabilizing the power rail during fast transients.

Circuit Design

This lab involves building the slammer circuit which involves using an op amp to create a slow edge rise and pin13 from an arduino uno as a fast edge. I will be building my circuit from this model:

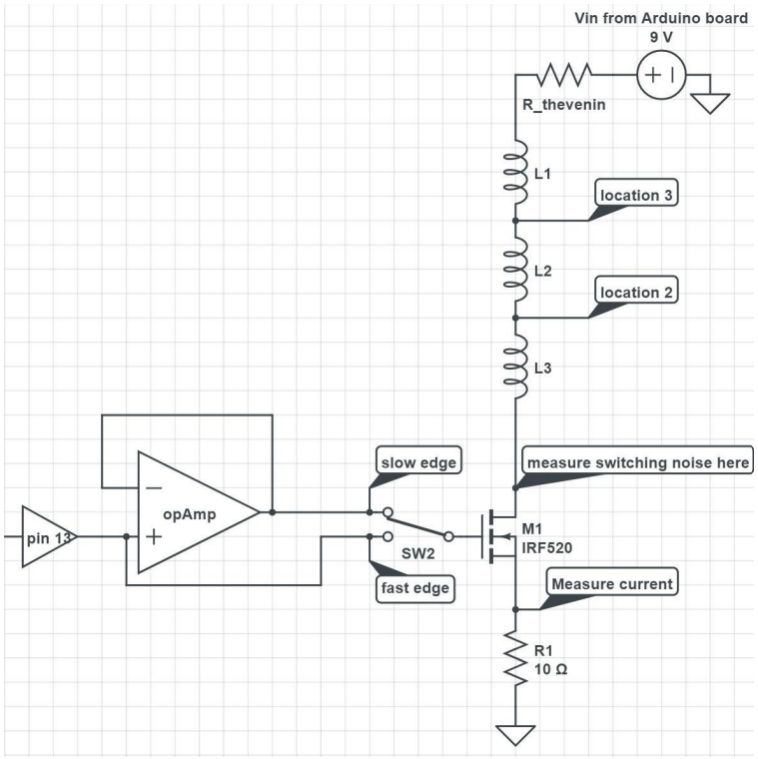

Figure 1: Slammer Circuit Diagram

From here we can build the circuit using best practices onto a sbb:

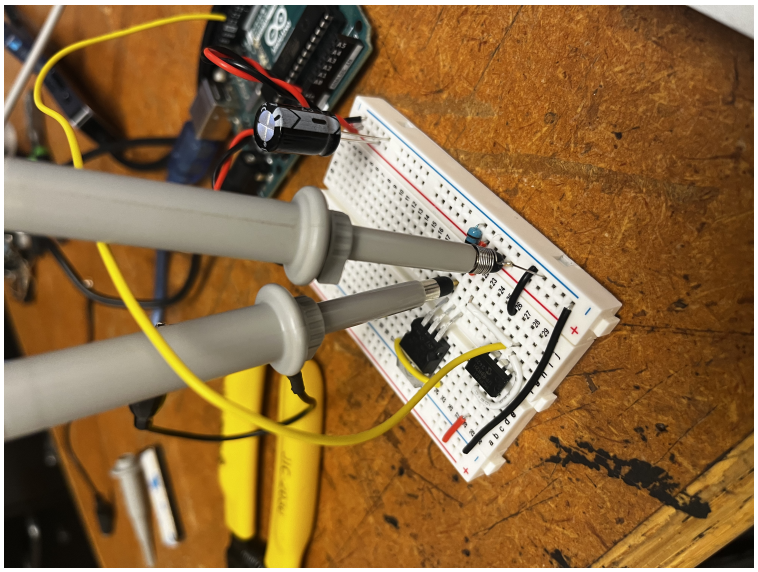

Figure 2: Circuit on SBB

From here we can verify that the pin13 duty cycle is less than 10%, we are shooting for 5%, so that the power across the resistor and mosfet are within safe bounds. Here are the graphs of the waveform as well as the rise time for both the fast edge from the arduino around 5ns and the slow edge from the op amp roughly 1.5us:

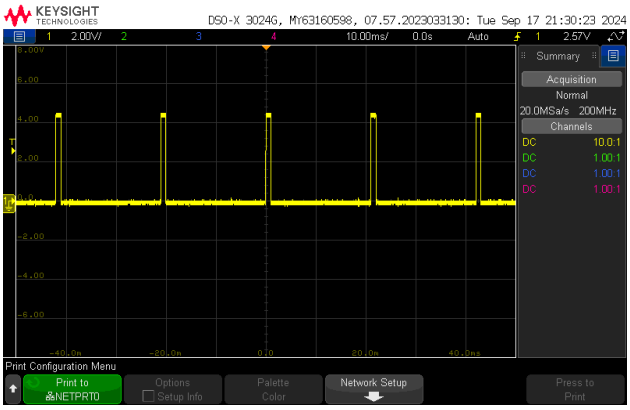

Figure 3: Pin 13 Waveform

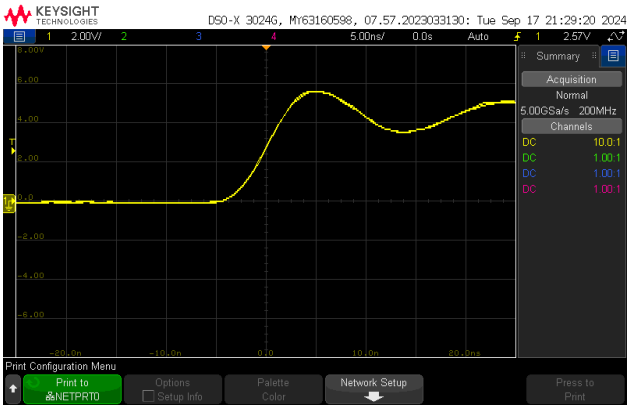

Figure 4: Fast Rise Time around 5ns

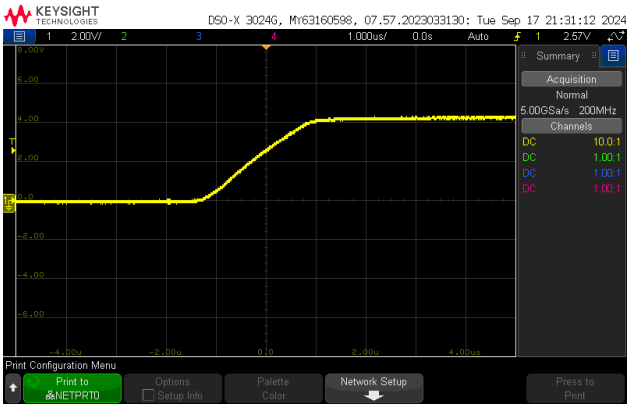

Figure 5: Slow Rise Time around 1.5us

Results

To show the impact of the switching noise we will show graphs of the switching noise with and without the decoupling capacitor and further, the difference between a large capacitance such as 1000uF and 1uF. We will also show the difference of having capacitors close to the IC and far away from the IC. I will be showing all of the figures with the fast edge.

Switching Noise - Decoupler Effect

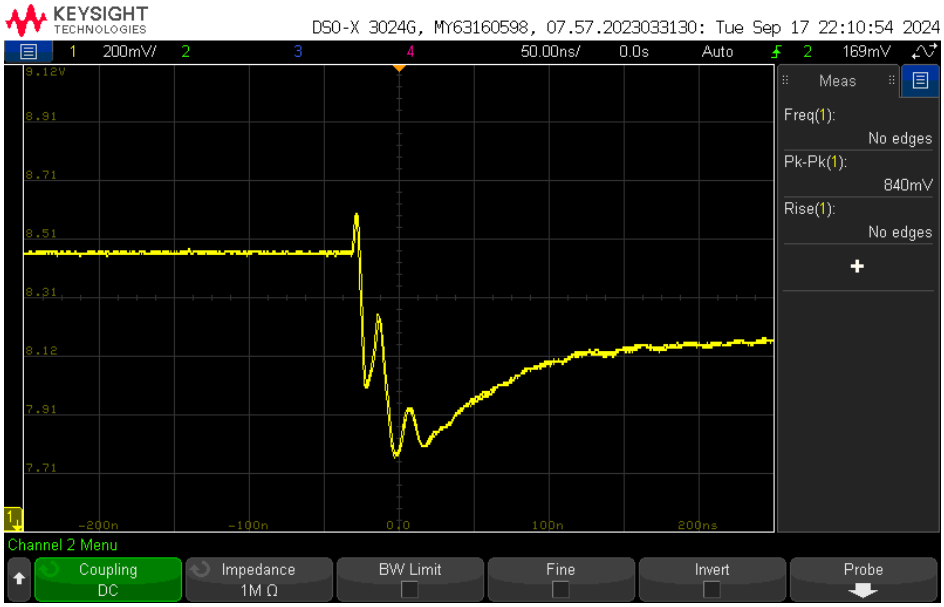

Figure 6: Switching Noise without Decoupling Capacitor

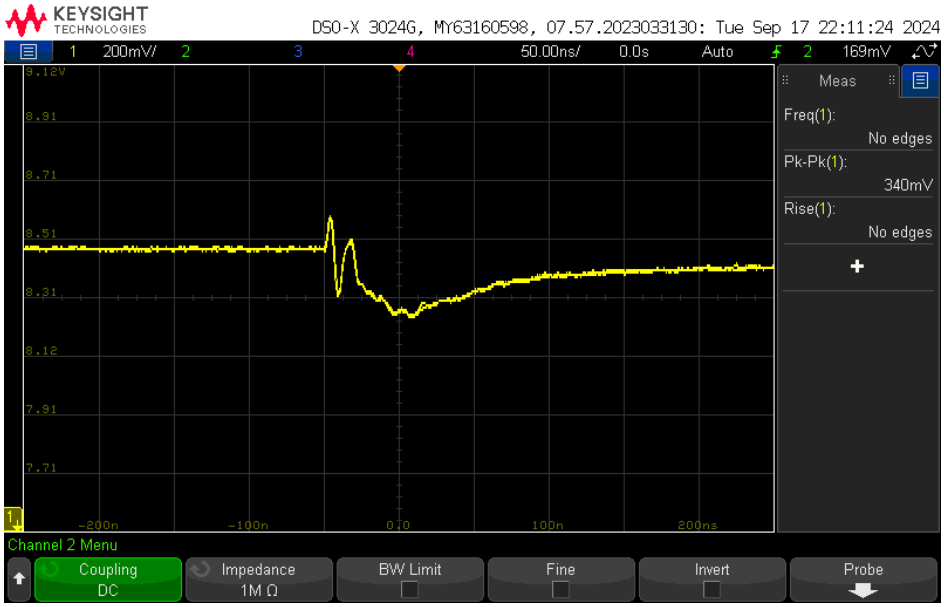

Figure 7: Switching Noise with 1000uF Decoupling Capacitor

These two figures show the impact of using a decoupling capacitor, the switching noise is dramatically reduced simply by adding a decoupling capacitor anyway along the power rails.

Switching Noise - Capacitance Effect

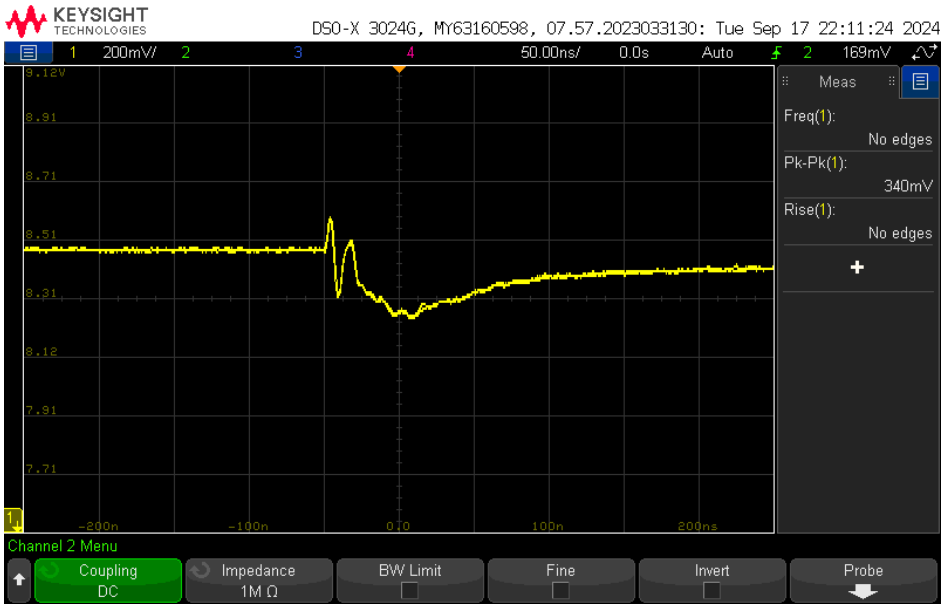

Figure 8: Switching Noise with 1000uF Decoupling Capacitor

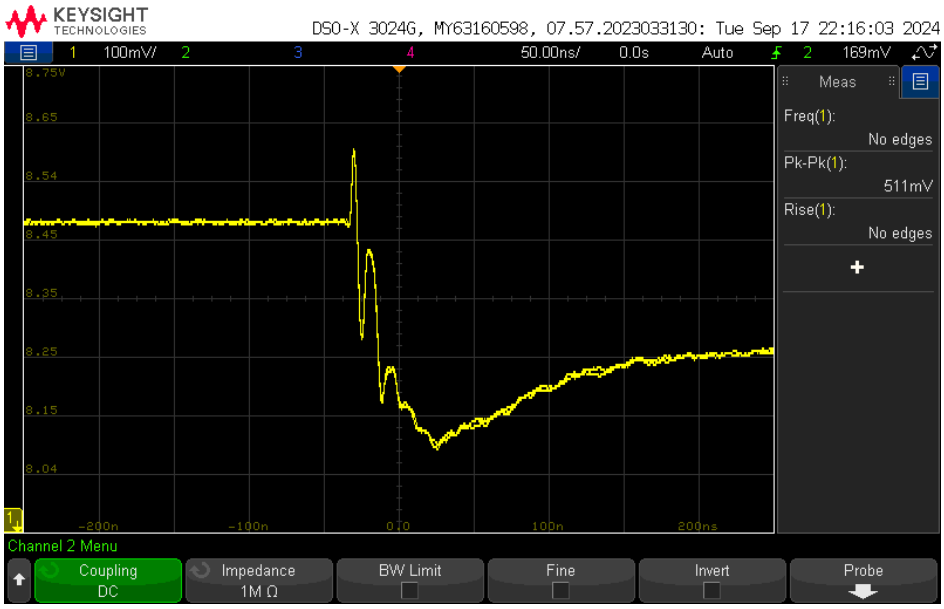

Figure 9: Switching Noise with 1uF Decoupling Capacitor

These two figures show the impact of the capacitance. Using the change of voltage across a capacitor equation and a current through the resistor of 0.4A (4V through 10ohms), and a desired voltage drop of less than 0.4V, and a rise time of 1uS we gather:

$$C = \frac{I * dt}{dV} = \frac{0.4 * 1\mu S}{0.4V} = 1\mu F$$

Figure 10: Capacitance Calculation

Switching Noise - Loop Inductance effect

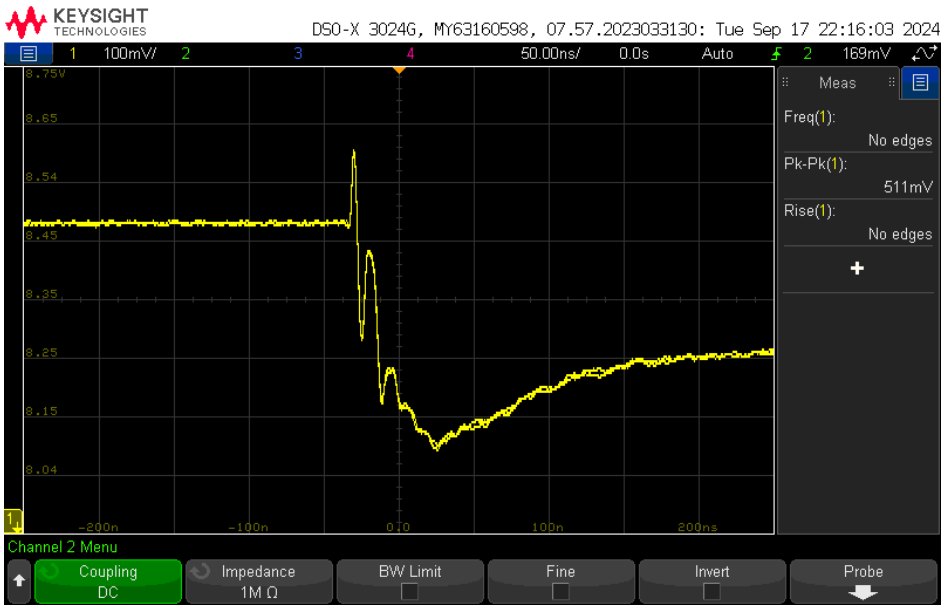

Figure 11: Switching Noise with 1uF Decoupling Capacitor Far away

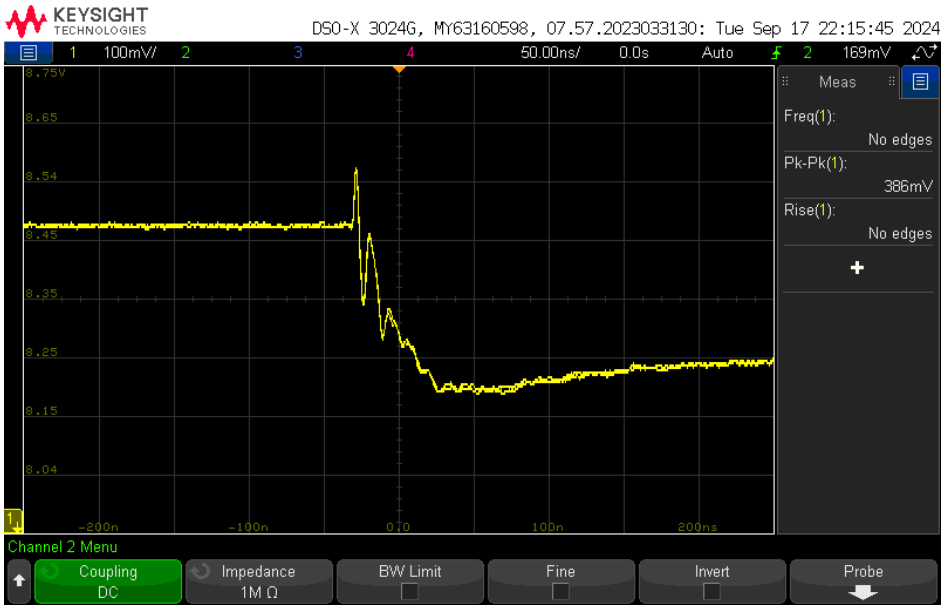

Figure 12: Switching Noise with 1uF Decoupling Capacitor Close

These two figures show the impact of the loop inductance. With the 1uF capacitor far away we have a larger amount of switching noise. This is due to the loop being larger, creating a stronger loop inductance.

Takeaways

We can calculate the thevenin resistance as the (thevenin voltage - load voltage)/load current. As stated previously we know the load current to be 0.4 amps because there is 4V through a 10ohm resistor. We know the thevenin voltage from the Vin pin of the arduino to be 9V. To find the load voltage we observe the voltage of figure 11 which is 8.5V. From here we can calculate the thevenin resistance to be 1.25ohms.

To calculate the loop inductance we can use the following relationship:

$$\Delta V = L\frac{dI}{dt}$$

Figure 13: Loop Inductance Calculations

From figure 11 we see the voltage drop to be 0.4V and again the current is 0.4A and the switching noise time to be 50ns, thus the loop inductance can be calculated as 0.4V/0.4A x 50nsec = 50nH. This calculation makes sense because for the rise time of roughly 2usec and the inductance of 50nH with a current of 0.4A we get 50nH x 0.4A / 2usec = 0.01V which is much smaller than the switcing noise of the fast rise time. Again this makes sense because the change of current is the same which means dI/dt is much larger for the fast rise time because the timescale is much smaller.

The design principles I learned from this lab show that not only do we need a decoupling capacitor with fast rise time circuits but that we need to choose the correct capacitance value based on our desired switching noise andf further most importantly that it needs to be close to the IC we are measuring to reduce cross talk and loop inductance.