University of Colorado - Boulder

ECEN 5730
Practical PCB Design Manufacture — Fall 2024

Board 2 and Lab 15 Report

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Introduction

This report presents the design, testing, and measurement results for **Board 2**, which focuses on the influence of good and bad PCB layout practices on switching noise, and **Lab 15**, where I compare results obtained from my board with the professor's pre-built version. Key topics include noise measurements on quiet high/low pins, rail compression, power consumption, and performance comparisons when powering the hex inverters with 3.3V and 5V.

Plan of Record (POR)

The Plan of Record for **Board 2** involves demonstrating the effects of good versus bad PCB layout design on switching noise. The primary goal is to compare noise levels and rail compression between the good and bad sections of the board. This includes measuring quiet high and quiet low signals on the hex inverters, analyzing switching noise on the power rails, and investigating power consumption differences when using 3.3V versus 5V rails.

What it Means for the Board to "Work"

For Board 2 to be considered functional, it must meet the following expectations:

- **Power Integrity**: The board must provide stable 5V and 3.3V power rails, with minimal ripple and noise on both rails. Voltage regulators should maintain these values under varying load conditions without significant drops or instability.
- **Signal Integrity**: The hex inverters must properly propagate signals with clear transitions between high and low states. The signal rise and fall times should be consistent with expected values, and the quiet high and quiet low signals should exhibit minimal noise.
- **Noise Control**: The good layout is expected to demonstrate significantly lower switching noise than the bad layout. This is particularly important on the quiet high and quiet low signals, as well as the 5V and 3.3V power rails. The bad layout, with poor grounding and suboptimal decoupling capacitor placement, will serve as a reference for higher noise levels.
- **Component Behavior**: The 555 timer should produce a clean output waveform with stable rise and fall times. Similarly, the hex inverters must maintain expected behavior under different operating conditions (e.g., switching between 3.3V and 5V rails).
- **Rail Compression**: The difference between the quiet high and quiet low signals (rail compression) should remain minimal on the good layout. The bad layout is expected to exhibit higher rail compression due to poor power delivery and layout practices.
- **Power Consumption**: Power consumption of the board, particularly on the hex inverters, should be within expected ranges for both 3.3V and 5V operation. Switching noise should not significantly impact power efficiency.

Project Overview

Block Diagram

The figure below shows the block diagram outlining the power conditioning, illustrating the flow of power (5V or 3.3V) to the LMC555 timer and the hex inverters.

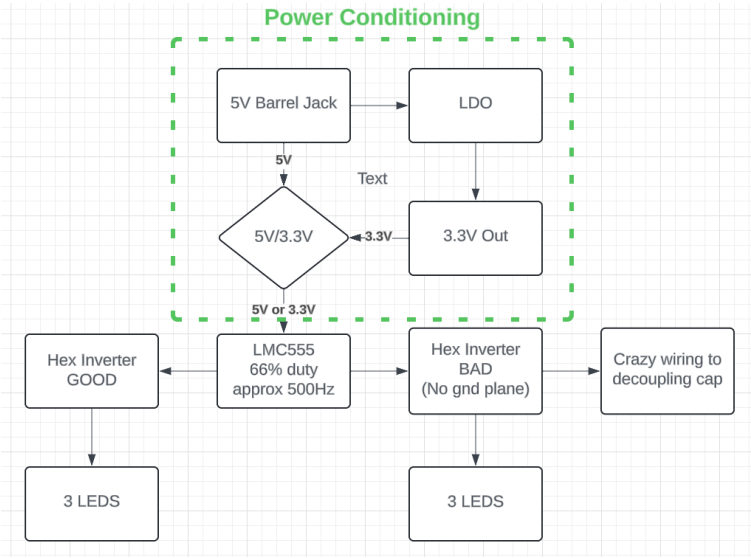

Figure 1: Block Diagram of Circuit

Block Diagram Sketch (Back of Napkin)

The figure below shows the rough sketch (back of napkin) of the hex inverter setup, outlining how the hex inverters are connected in the circuit for the power rail noise tests.

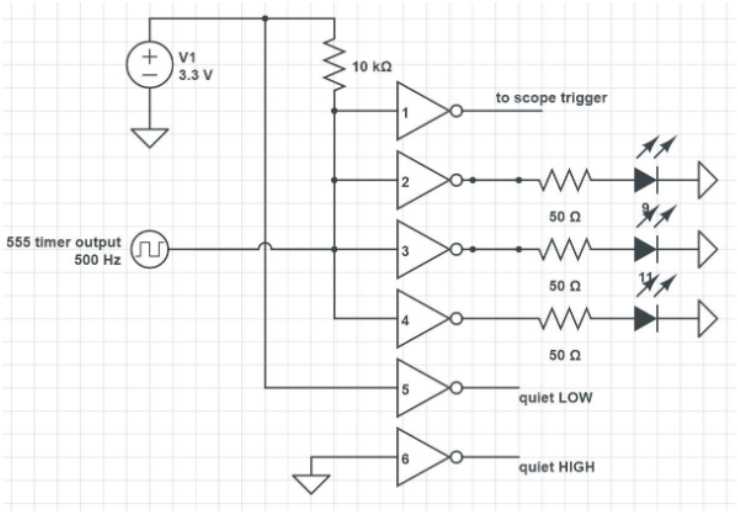

Figure 2: Back of Napkin Sketch of Hex Inverter Setup

Schematic in Altium Designer

The figure below presents the schematic created in Altium Designer. Both the good and bad layouts share the same basic components, including the LMC555 timer (note: the diagram includes a NE555, however the LMC and NE have the same footprint so I designed this board to be used with the LMC555) and two hex inverters, but the routing and layout differ significantly.

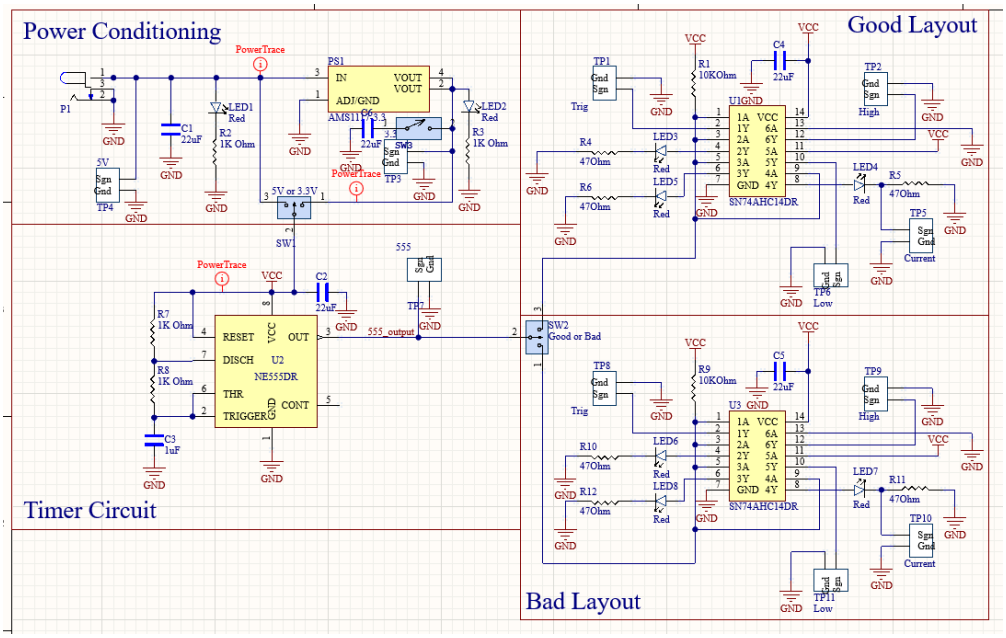

Figure 3: Schematic in Altium Designer

PCB Layout

The PCB layout shows the good and bad layout regions. The bad layout lacks a continuous ground plane, and the decoupling capacitor is very poorly placed as well as routed with the most zigzags of any trace, resulting in increased noise.

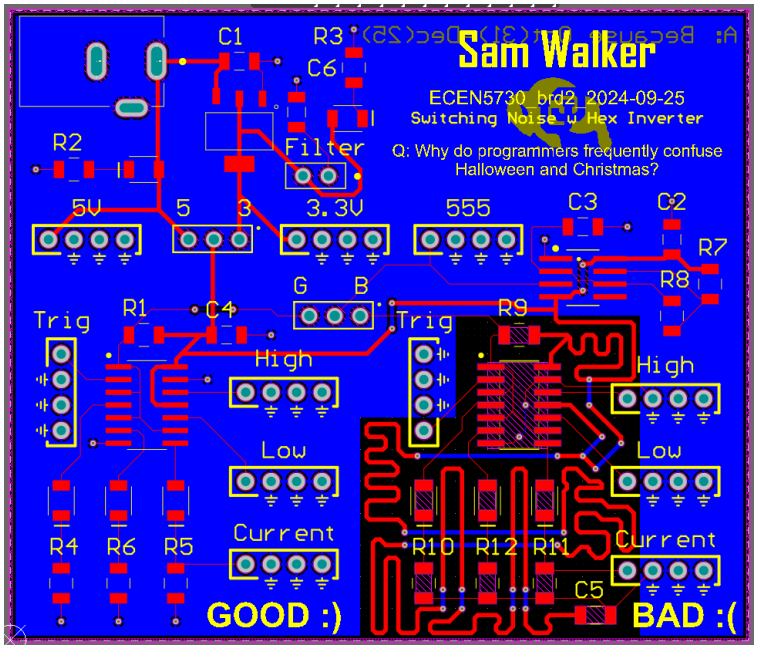

Figure 4: PCB Layout

Professor's Board (Good-Good, Good-Bad, and Bad-Bad Layouts)

The figure below shows my professor's board, which contains three distinct layout regions: the good-good layout, the good-bad layout, and the bad-bad layout. Each layout provides a unique comparison of how various design practices (continuous ground plane, decoupling placement, etc.) affect switching noise and power rail performance. This board serves as the reference for comparing different noise levels on quiet high/quiet low signals and power rails.

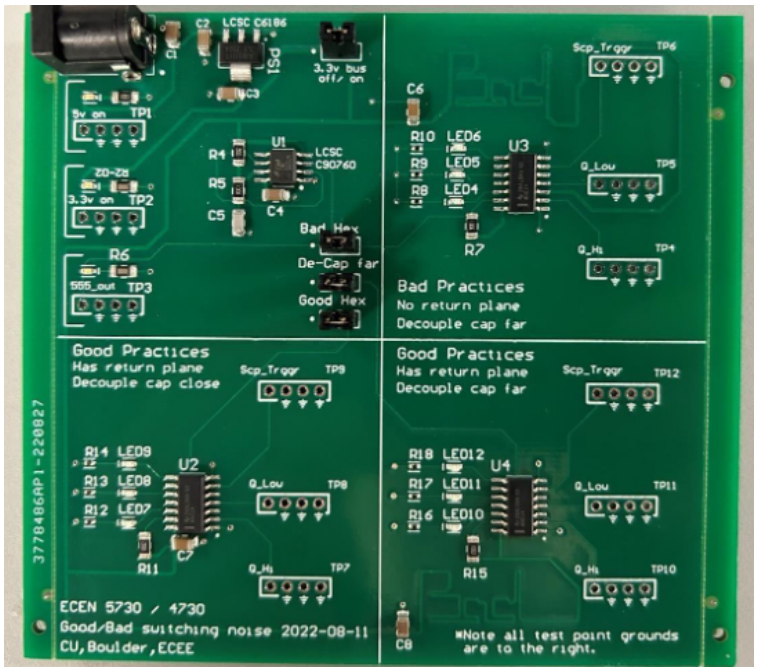

Figure 5: Professor's Board Showing Good-Good, Good-Bad, and Bad-Bad Layouts

Unassembled Board (JLCPCB)

The figure below shows my unassembled Board 2 as received from JLCPCB. This image shows the board without any components soldered onto it, allowing us to visualize the routing and overall design before the testing phase.

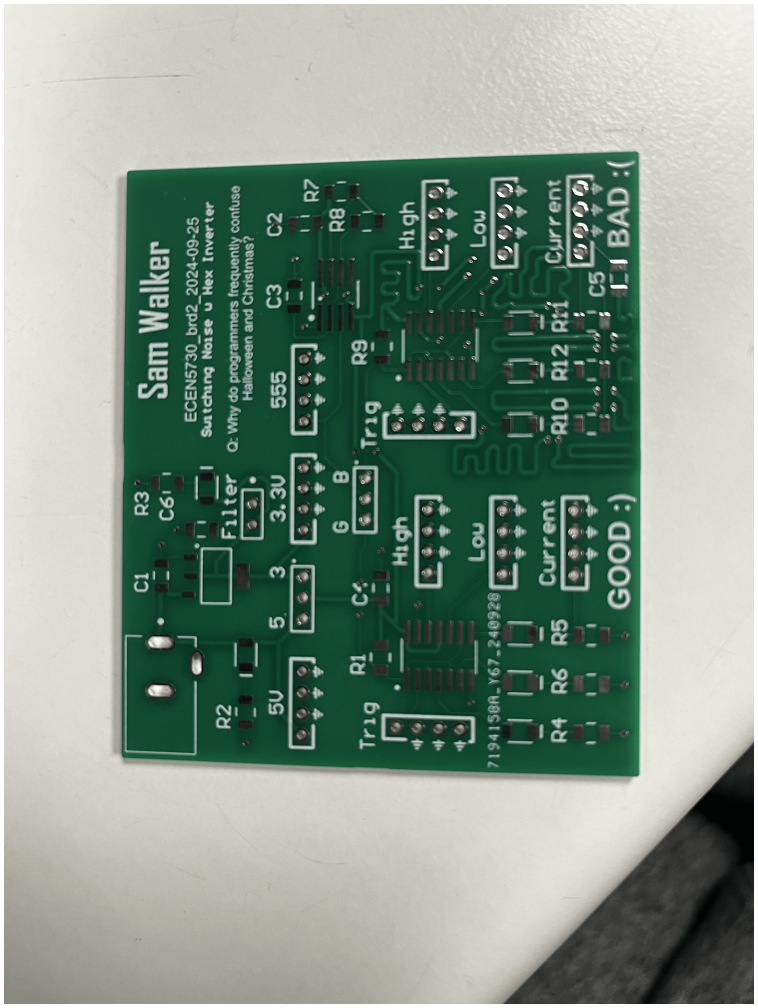

Figure 6: Unassembled Board from JLCPCB

Assembled Board (With Components)

The figure below shows my fully assembled Board 2 with all components soldered. Key components include the LMC555 timer, the hex inverters, and decoupling capacitors. This board was tested under various conditions to compare the good and bad layouts, focusing on switching noise and power rail performance.

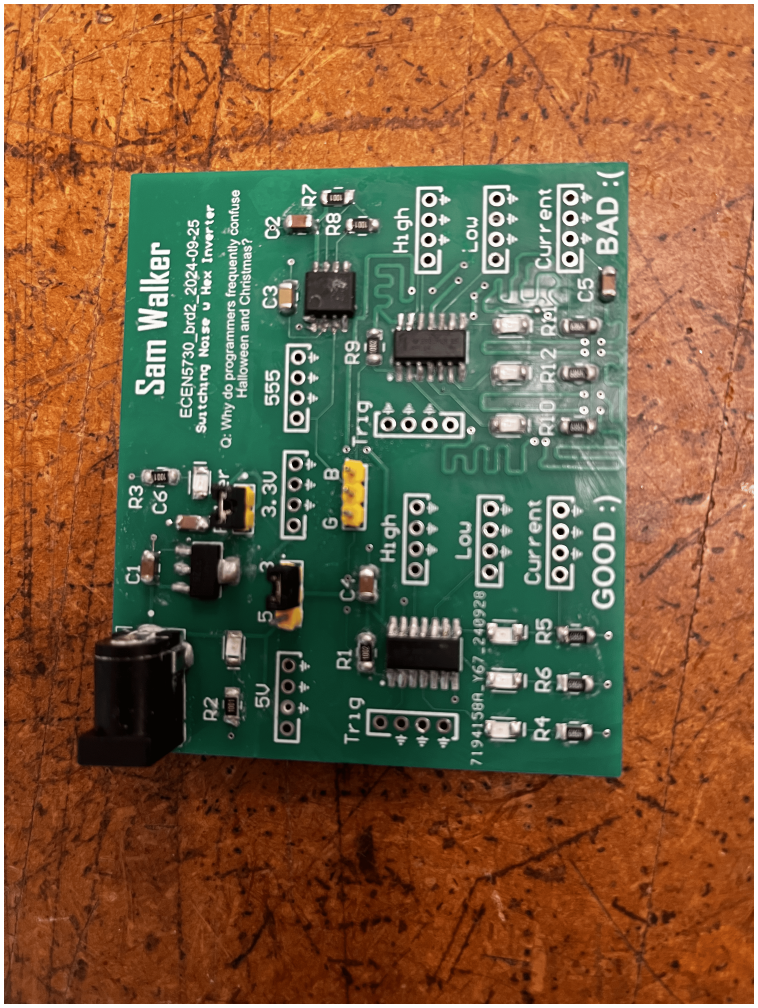

Figure 7: Assembled Board with Components

Board 2 Testing and Measurements, Compared to Lab 15 Board

555 Timer Output

The figures below show the 555 timer output on my board compared to my professor's board. On my board, the rise time is measured at 516 nanoseconds, with some unexpected overshoot behavior, as seen in the first figure below. In comparison, the signal on the professor's board was cleaner, with only a 37 nanosecond rise time, as shown in the second figure. I believe this discrepancy in rise time is due to the different 555 timers used: my professor likely used a TLC555, whereas I used an LMC555, which is known to exhibit slower rise times under similar conditions.

Exploring the 555 outputs deeper, we can compare the frequencies and duty cycles between my board and the professor's board.

Frequency and Duty Cycle Comparison:
On my board (third figure below), the 555 timer produces a signal with a frequency of 494 Hz and a duty cycle of 65.5%. This is close to the target frequency of 500 Hz but shows some variation in the duty cycle, likely due to the overshoot behavior observed in the rise time. On the professor's board (fourth figure below), the frequency is 981.5 Hz, with a duty cycle of approximately 34%. This discrepancy is due to different component values used in the timing circuit, resulting in a faster oscillation and different duty cycle compared to my board.

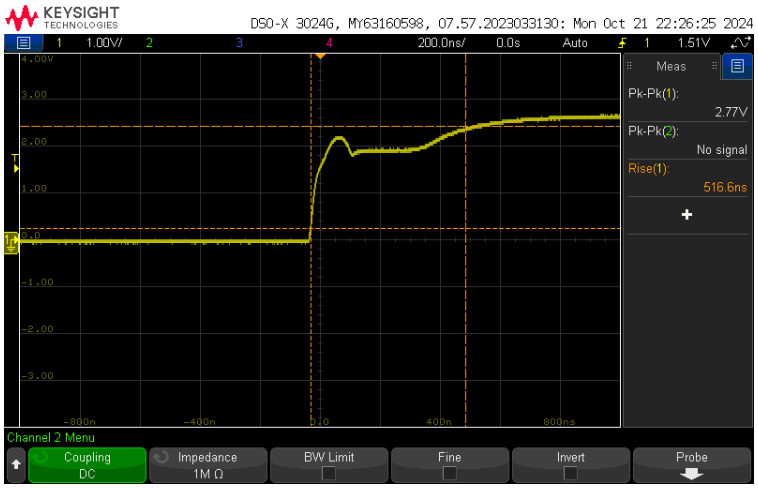

Figure 8: 555 Timer Output on My Board (Rise Time)

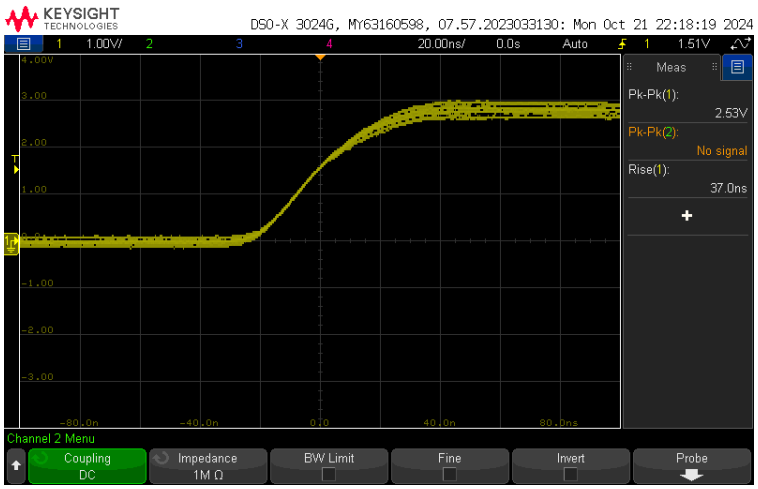

Figure 9: 555 Timer Output on Professor's Board (Rise Time)

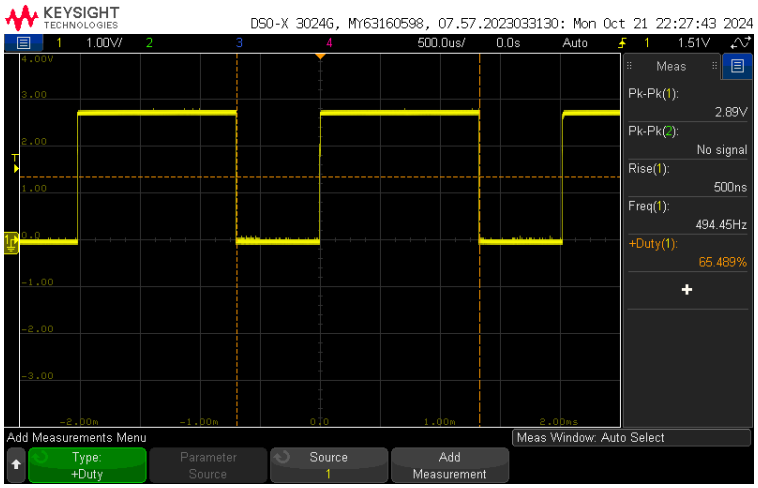

Figure 10: 555 Timer Frequency and Duty Cycle on My Board

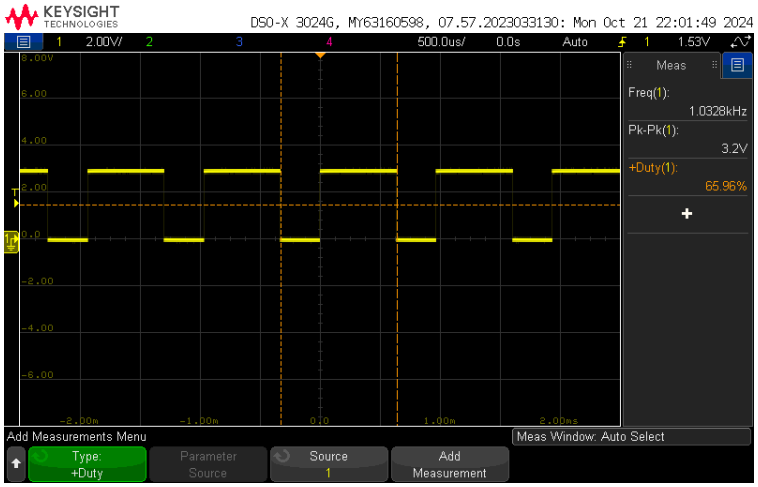

Figure 11: 555 Timer Frequency and Duty Cycle on Professor's Board

In summary, my board shows a slower rise time and a frequency slightly under 500 Hz, while the professor's board has a much faster signal with a frequency closer to 1 kHz. The different timing components and 555 timer models (LMC555 vs. TLC555) are likely responsible for these variations, as well as the different resistor and capacitor choices affecting the frequency.

Scope Trigger Waveform

The figures below show the scope trigger waveform from both my board and my professor's board. On my board (first figure), the waveform has a 34% duty cycle, similar to the result from Lab 15, but slightly different from the expected value.

On my professor's board (second figure), the waveform also has a 34% duty cycle. The main difference between the two waveforms lies in the frequency, which is higher on the professor's board due to the faster oscillation from the different 555 timer model (TLC555 vs. LMC555). This difference in frequency is expected, as it stems from the previously observed difference in the 555 timer outputs.

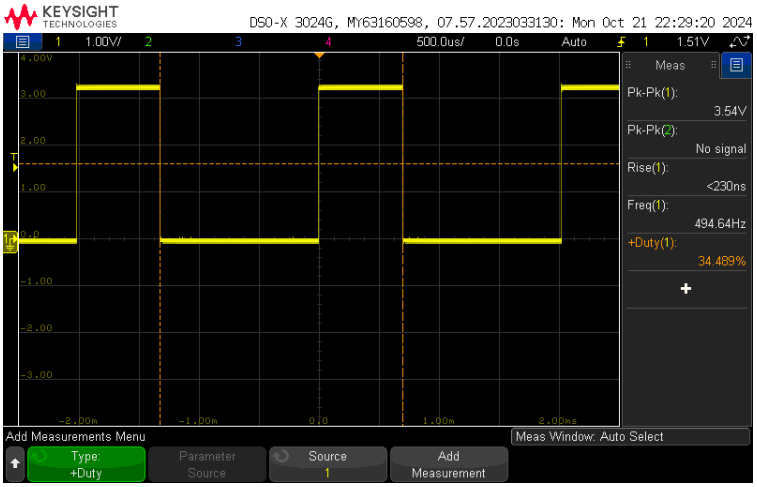

Figure 12: Scope Trigger Waveform on My Board

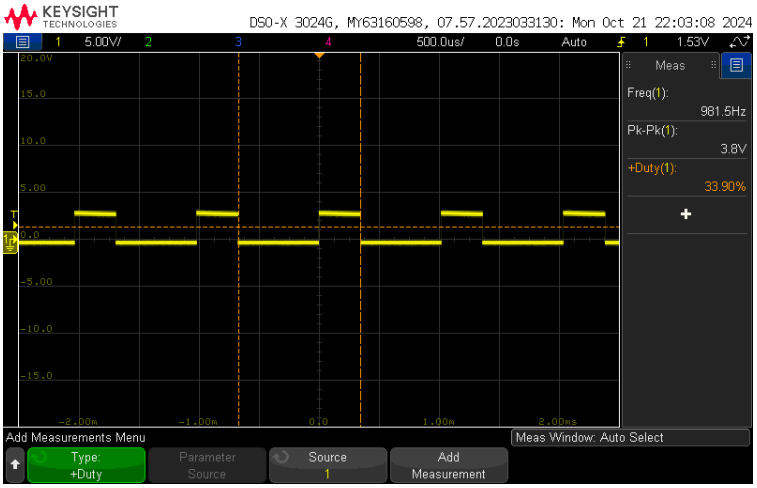

Figure 13: Scope Trigger Waveform on Professor's Board

Both waveforms are identical in terms of duty cycle and overall shape, confirming that the difference in frequency is a direct consequence of the different timing components used in each board's circuit.

Quiet High and Quiet Low Noise

The figures below show the noise levels on the quiet high and quiet low signals for both the good and bad layout regions. As expected, the good layout demonstrates significantly lower noise compared to the bad layout, which suffers from poor design practices such as a removed ground plane and poorly placed decoupling capacitors.

Good Layout Analysis: In the good layout (first figure), the quiet high signal experiences a noise level of around 336 mV, while the quiet low shows significantly less noise at 57.8 mV. This difference can be attributed to the fact that the quiet high signal is more susceptible to noise because it sits closer to the power rail (Vcc). The inductance in the power delivery network (PDN), especially on poorly designed boards, causes more voltage fluctuations at the higher signal level (quiet high). This is exacerbated when switching transitions occur, leading to a higher noise amplitude on quiet high compared to quiet low, which remains closer to ground and is less impacted by PDN fluctuations.

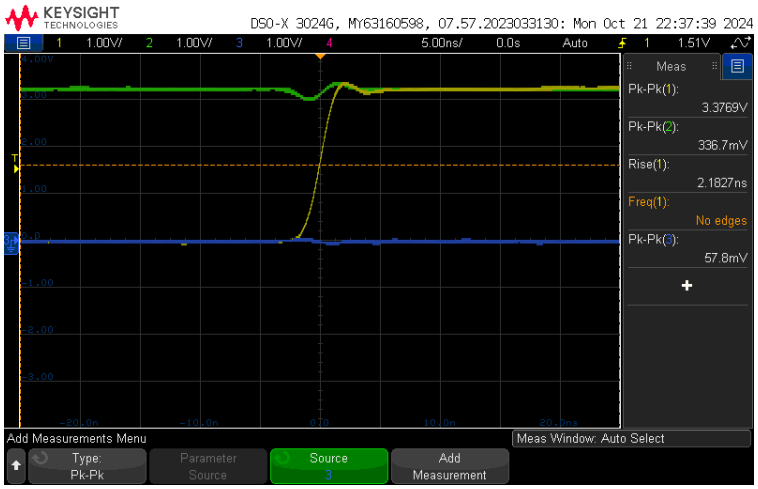

Figure 14: Quiet High and Low Noise on Good Layout (336 mV vs. 57.8 mV)

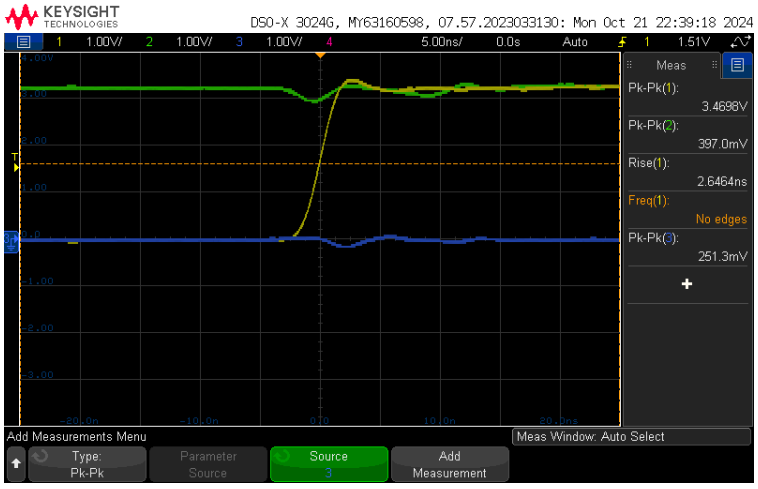

Figure 15: Quiet High and Low Noise on Bad Layout (397 mV vs. 251 mV)

Bad Layout Analysis: In the bad layout (second figure), the noise is considerably worse, with the quiet high showing 397 mV of noise and the quiet low exhibiting 251 mV. This increase in noise is due to several factors:

Missing Ground Plane: The bad layout lacks a continuous ground plane, which means the return current paths are longer and less direct, resulting in higher parasitic inductance and greater noise susceptibility.

Poor Decoupling Capacitor Placement: The decoupling capacitors are placed far away from the IC pins, which reduces their effectiveness in filtering noise. This results in higher noise on both the quiet high and quiet low signals because the capacitors are unable to smooth out rapid voltage changes caused by switching transitions.

Comparison with Lab 15 (Good-Good and Bad-Bad Layouts): Similar results were observed on my professor's board in Lab 15, where we compared the quiet high and quiet low noise in both the good-good and bad-bad layouts. The good-good layout in Lab 15 showed low noise levels, similar to the good layout on my board, with approximately 320 mV on the quiet high and 50 mV on the quiet low (Figure below). This reinforces the idea that well-designed boards with continuous ground planes and properly placed decoupling capacitors can significantly reduce noise.

In contrast, the bad-bad layout on the professor's board displayed even worse noise characteristics, with around 680 or 320 mV of noise on the quiet high and 400 or 50 mV on the quiet low (Figure below). This closely mirrors the behavior on my board's bad layout and highlights how poor design choices, such as a lack of ground plane and improper decoupling, lead to severe degradation in signal quality and increased noise.

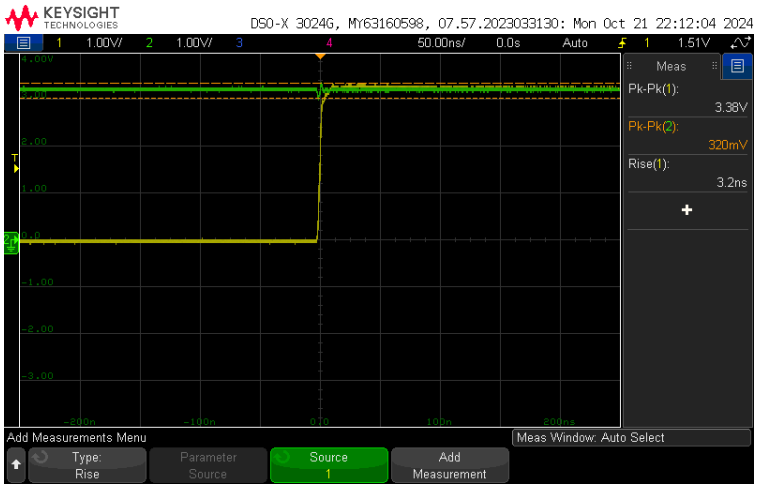

Figure 16: Quiet High on Good-Good Layout (320 mV)

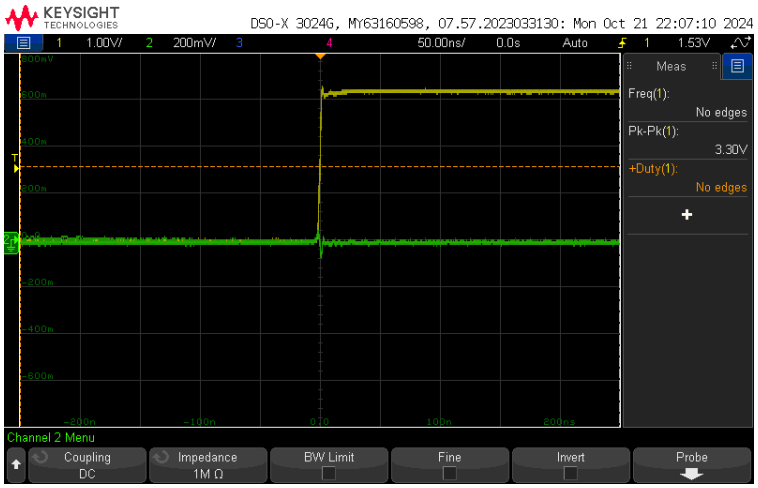

Figure 17: Quiet Low on Good-Good Layout (50 mV)

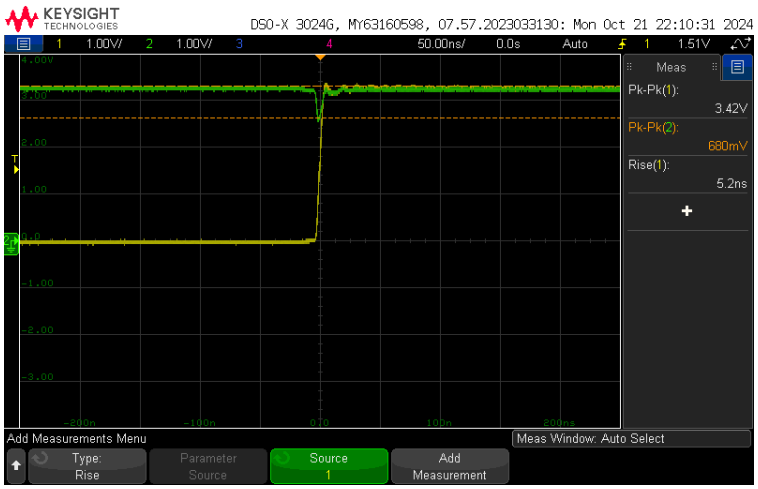

Figure 18: Quiet High Low on Bad-Bad Layout (680 mV)

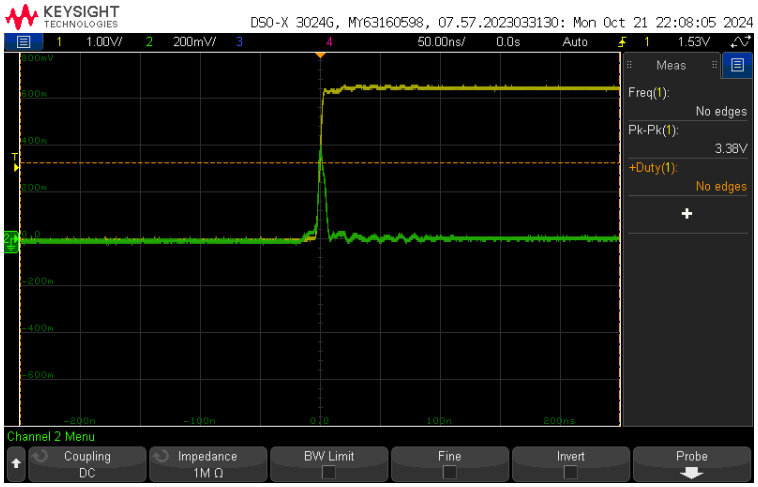

Figure 19: Quiet Low on Bad-Bad Layout (400 mV)

Power Rail Noise

The figures below show the switching noise on the 5V and 3.3V rails from my board. On my board, the 3.3V rail exhibits about 40 mV of noise, which is higher than expected, while the 5V rail shows only 21 mV of noise. The relatively low noise on the 5V rail can be attributed to proper decoupling and a continuous ground plane in the good layout.

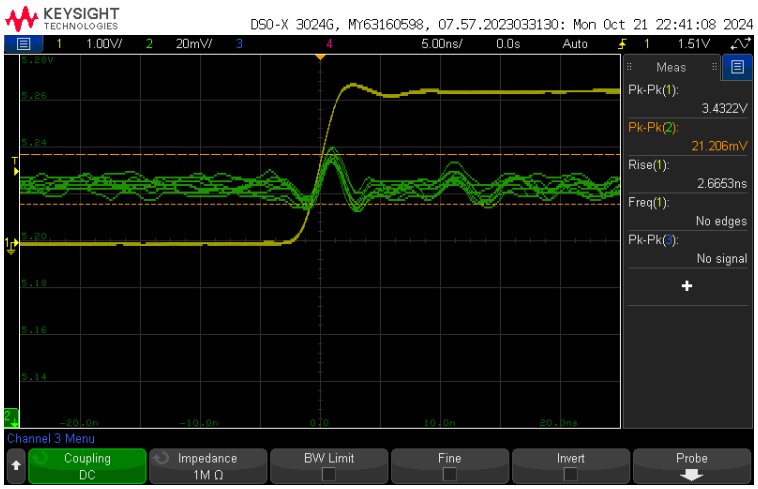

Figure 20: 5V Rail Noise on My Board (21 mV)

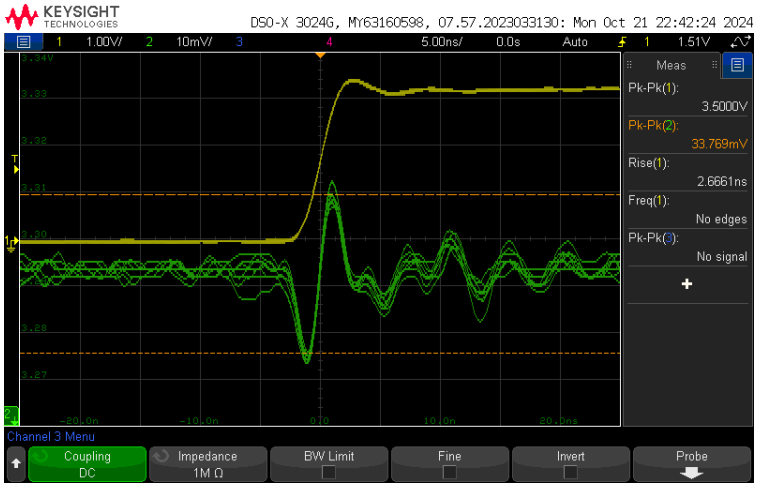

Figure 21: 3.3V Rail Noise on My Board (40 mV)

Comparison with Professor's Board: On my professor's board, the noise levels on both the 5V and 3.3V rails were significantly higher. For the 5V rail (Figure below), the noise measured around 80 mV, while the 3.3V rail (second figure below) showed 100 mV of noise. This increase in noise compared to my board is likely due to differences in the power delivery network and decoupling capacitor effectiveness. Additionally, the professor's board may have more components drawing current, leading to higher switching noise on both power rails.

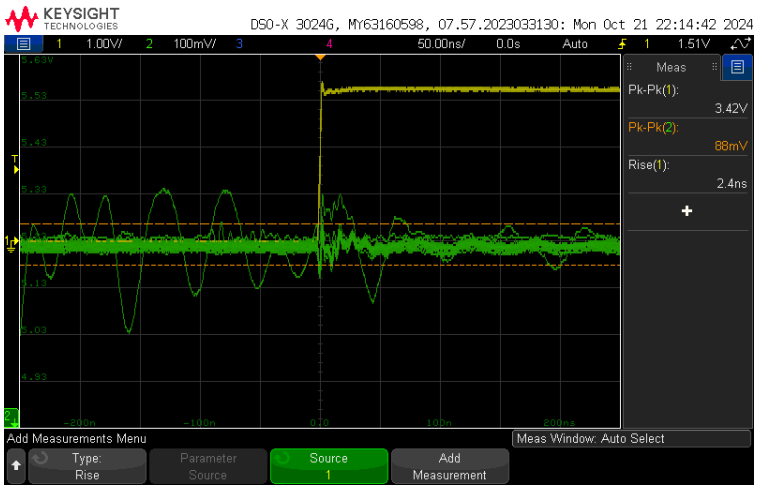

Figure 22: 5V Rail Noise on Professor's Board (88 mV)

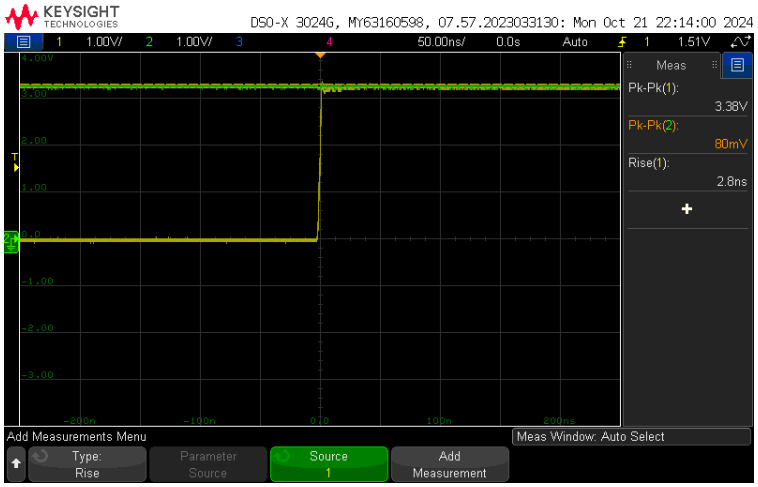

Figure 23: 3.3V Rail Noise on Professor's Board (80 mV)

Overall, the noise levels on my board's power rails are much lower than those observed on my professor's board, especially on the 3.3V rail, where my board exhibited less than half the noise. This suggests that the layout and decoupling strategies employed on my board were effective in minimizing switching noise.

Rail Compression

Rail compression refers to the change in voltage between the quiet high and quiet low signals on the hex inverter die, which reflects the actual voltage seen between Vcc and GND. By subtracting the quiet high and quiet low signals using a scope's math function, the rail compression can be observed.

In my measurements, the rail compression on the bad layout was about 1.5V peak-to-peak, while the good layout reduced this to 858.4 millivolts.

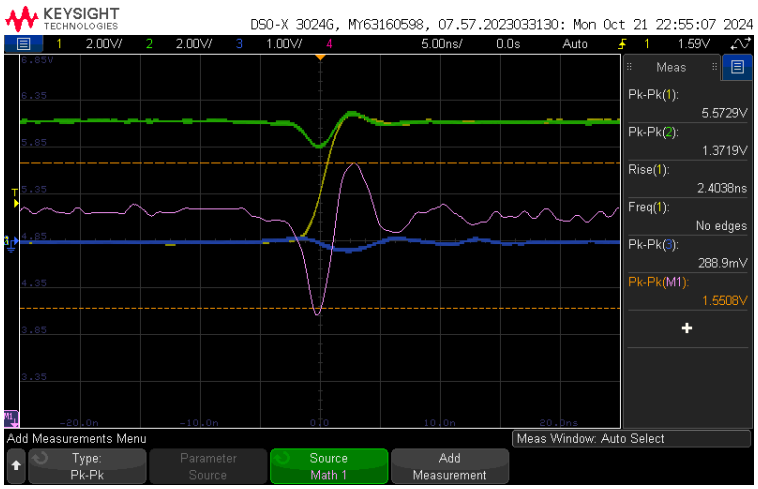

Figure 24: Rail Compression on Bad Layout (1.5V peak-to-peak)

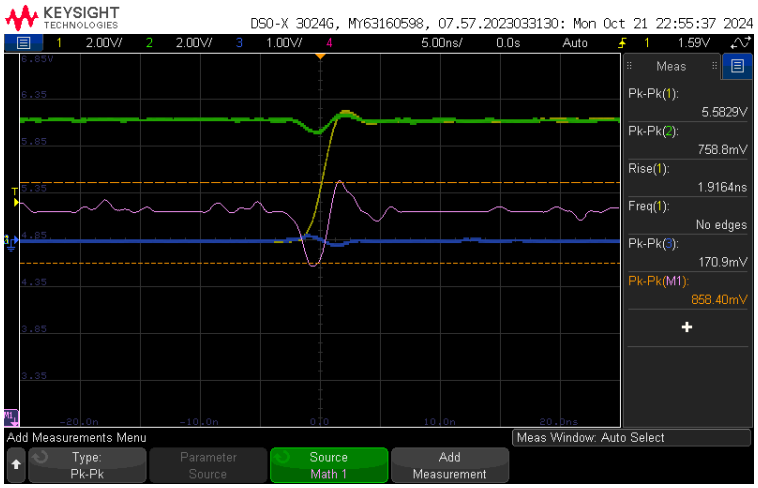

Figure 25: Rail Compression on Good Layout (858.4 mV peak-to-peak)

Comparison of 3.3V vs. 5V Powering the Hex Inverter

The figure below compares the quiet low noise levels when powering the bad hex inverter with 3.3V versus 5V. The 5V power rail shows about 300 millivolts more noise compared to the 3.3V rail. This increase in noise can be attributed to the higher voltage supplied to the hex inverter, which leads to larger fluctuations and more energy in the switching transitions, resulting in greater noise.

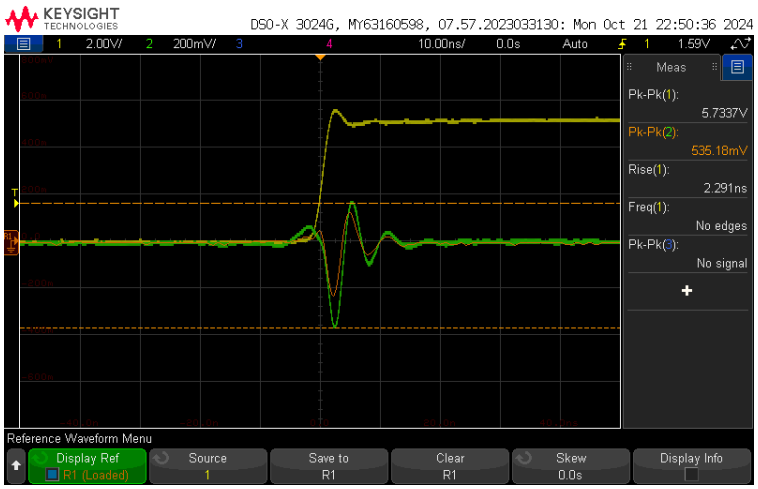

Figure 26: Comparison of 3.3V vs. 5V Powering the Hex Inverter

In terms of signal rise time, the figure below shows the measurement of the scope trigger rise time when powered by both 5V and 3.3V. Interestingly, the rise time remains the same for both 5V and 3.3V, which is expected because the switching speed of the hex inverter is largely determined by the internal properties of the device, not the supply voltage. Both voltages provide sufficient headroom for fast switching, and thus, the rise time does not vary significantly.

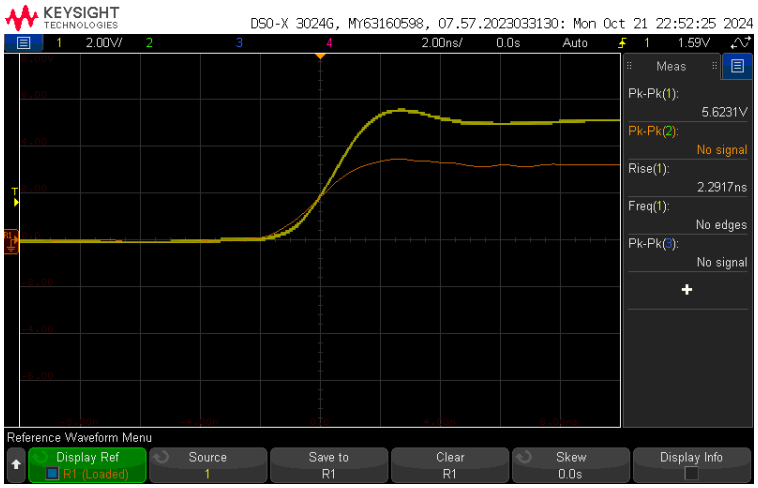

Figure 27: Scope Trigger Rise Time on 5V vs. 3.3V Power

The difference in noise, however, can be explained by the fact that higher voltages inherently generate more noise due to greater energy transfer during switching. The higher 5V rail leads to more pronounced voltage swings, which increases the noise observed on the quiet low signal, while the lower 3.3V rail results in less pronounced noise.

Thevenin Output Resistance of the Hex Inverter I/O

Using the current measurements across the 47ohm resistor, we can estimate the Thevenin output resistance of the hex inverter without altering the circuit.

1. **No-Load Voltage (V_{oc})**: The no-load voltage, V_{oc}, can be approximated as the power supply voltage, which in this case is 5V.

2. **Loaded Voltage Calculation**: Using the current measured across the 47ohm resistor, we can calculate the loaded voltage. According to Ohm's law:

$$V_{load} = I_{load} \times R_{load}$$

From my current measurement, $I_{load} \approx 12.77\,\text{mA}$ across the 47ohm resistor. Therefore:

$$V_{load} = 12.77\,\text{mA} \times 47\,\Omega \approx 0.60\,V$$

3. **Thevenin Resistance Calculation**: Using the calculated loaded voltage and the no-load voltage, the Thevenin resistance can be estimated as:

$$R_{th} = R_{load} \times \left(\frac{V_{oc} - V_{load}}{V_{load}} \right)$$

Substituting the values:

$$R_{th} = 47\,\Omega \times \left(\frac{5V - 0.60V}{0.60V} \right) \approx 348.3\,\Omega$$

The calculated Thevenin output resistance of approximately 348.3ohms. While this is a rough estimate, it highlights the importance of considering the real-world performance of the hex inverter in circuit configurations where output impedance affects signal behavior.

Further analysis with different load conditions could refine this estimate, but the current measurement provides a useful approximation of the Thevenin output resistance in this configuration.

What Worked

Definition of What It Means to Work

For Board 2 to be considered functional, it must meet the expectations outlined in the Plan of Record (POR). This includes the following:

- **Power Integrity**: The board should provide stable 5V and 3.3V power rails with minimal ripple and noise.
- **Signal Integrity**: The hex inverters must propagate signals with proper transitions between high and low states, with expected rise and fall times.
- **Noise Control**: The good layout should exhibit significantly lower switching noise compared to the bad layout, particularly on the quiet high/quiet low signals and the power rails.
- **Component Behavior**: The 555 timer should output a stable waveform with proper rise and fall times, while the hex inverters must function consistently under different conditions.
- **Rail Compression**: The difference between the quiet high and quiet low signals (rail compression) should remain minimal in the good layout, with increased compression expected in the bad layout.
- **Power Consumption**: The board's power consumption should remain within expected ranges for both 3.3V and 5V operations.

Performance Features and What I Measured

To verify that the board met these expectations, I conducted several tests, which are detailed in various sections of this report:

- **Power Integrity**: As shown in the *Power Rail Noise* section, my board maintained stable 5V and 3.3V rails, with noise levels of 21 mV and 40 mV respectively, both of which were lower than the noise levels observed on the professor's board (80 mV on 5V and 100 mV on 3.3V).
- **Signal Integrity**: The rise times of the signals were measured in the *555 Timer Output* and *Scope Trigger Waveform* sections. The rise time for the 555 timer on my board was 516 ns, with clean signal transitions, while the professor's board achieved faster rise times due to the TLC555.
- **Noise Control**: The quiet high and quiet low signals were measured in the *Quiet High and Quiet Low Noise* section. The good layout on my board exhibited significantly lower noise (336 mV vs 57.8 mV) compared to the bad layout (397 mV vs 251 mV). These results were in line with the expectations for noise control.
- **Component Behavior**: The 555 timer and hex inverters functioned as expected under both 5V and 3.3V operations, as noted in the *Comparison of 3.3V vs. 5V Powering the Hex Inverter* section. Rise times remained consistent, and switching behavior was stable.
- **Rail Compression**: Rail compression was assessed by measuring the voltage difference between the quiet high and quiet low signals. The bad layout demonstrated more compression, as expected, due to poor layout practices.
- **Power Consumption**: In the *Power Consumption* section, the total power consumed by the board was calculated to be approximately 63.2 mW, after accounting for the duty cycle and current drawn through the LEDs.

Best Design Practices

Throughout the design of Board 2, I adhered to several best practices:

- **Ground Plane Continuity**: In the good layout, I ensured the use of a continuous ground plane, which minimized return path inductance and reduced switching noise. In contrast, the bad layout lacked this feature, resulting in higher noise.
- **Proper Decoupling Capacitor Placement**: Decoupling capacitors were placed close to the IC pins in the good layout to filter noise effectively. In the bad layout, the capacitors were placed far from the pins, leading to increased noise on the quiet high/quiet low signals.
- **Minimized Trace Lengths**: I kept trace lengths as short as possible in the good layout to reduce parasitic inductance and resistance, improving overall signal integrity.

What Did Not Work

There were a few aspects that did not meet the initial expectations:

- **Rise Time of the 555 Timer**: While the signal transitions were stable, the rise time for the LMC555 timer on my board was slower than expected at 516 ns, compared to the faster rise time of 37 ns observed on the professor's board using the TLC555.
- **Noise on the 3.3V Rail**: While the 3.3V rail on my board exhibited less noise than the professor's board, the 40 mV measured was still higher than expected.

Analysis of My Project

What Worked and Will Be Carried Forward

Several aspects of this project worked well and will be incorporated into future designs:

- **Ground Plane Design**: The good layout demonstrated the importance of maintaining a continuous ground plane. The noise levels on the quiet high and quiet low signals were significantly lower than in the bad layout, confirming that this is a best practice I will continue to use in future designs.
- **Decoupling Capacitor Placement**: Proper placement of decoupling capacitors, as observed in the good layout, helped reduce noise and ensure stable power delivery to the hex inverters and other components. This strategy will be used in future designs to maintain signal integrity and reduce noise.
- **Component Behavior**: The 555 timer and hex inverters performed as expected, especially in terms of stable switching behavior. The successful use of both 5V and 3.3V power rails demonstrated the flexibility of the design, which I plan to continue exploring.

What Did Not Work and What Will Be Done Differently

While the project was largely successful, a few areas did not work as expected, and these will be improved in future designs:

- **Labeling of Components**: During assembly, it became difficult to quickly identify resistor and capacitor values without labels on the board. In future designs, I will ensure that the values are labeled directly on the PCB, making assembly easier and more efficient.
- **Switch and Hex Inverter Issue (Soft Error)**: One notable issue was that the hex inverters remained powered even when the switch was in the "off" position. Initially, I could not determine the cause, but the issue resolved itself overnight. I suspect this was due to a small short on the switch pins, which corrected itself over time. No components were damaged, but in the future, I will ensure better switch pin routing to avoid such intermittent shorts.
- **Filter Capacitor LED Issue (Soft Error)**: Another soft error occurred when the LED connected to the filter capacitor remained on, even when the switch was off. This was due to incorrect routing of the capacitor, which was still connected despite the switch being off. This routing issue will be corrected in future designs to ensure that the capacitor is properly disconnected when the switch is off.

Soft Errors

The two soft errors in this project were:

- **Filter Capacitor LED**: The LED stayed on even when the switch was off due to improper routing of the filter capacitor. The capacitor remained connected regardless of the switch's state. I will correct this in future designs by ensuring that all components are properly disconnected when the switch is off.
- **Hex Inverter Power Issue**: The hex inverters were powered whether the switch was connected or not. This issue fixed itself overnight, which suggests it was likely caused by a tiny short on the switch pins. In future designs, I will pay extra attention to routing near the switch to prevent these kinds of shorts.

Hard Errors

There were no hard errors in this project, and no components were damaged during the design, assembly, or testing phases.

Future Design Improvements

In future designs, I plan to label resistor and capacitor values directly on the PCB to make the assembly process easier. Additionally, I will ensure that switches are properly routed to avoid the power issues observed in this project and prevent accidental shorts.

Conclusion

Both Board 2 and Lab 15 highlight the significance of PCB layout in managing switching noise and power integrity. The good layout on my board outperformed the bad layout, showcasing the value of proper design practices. Comparing my board with the professor's board also provided insight into areas for improvement, particularly with signal rise times and power rail noise. The analysis of power consumption and rail compression further emphasizes the importance of design optimization.